Notice of Allowability	Application No.	Applicant(s)	
	10/663,986	HUFF ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the filing of the application papers on 17 September 2003*.

2. ☒ The allowed claim(s) is/are *56-98 and 204-257*.

3. ☒ The drawings filed on *17 September 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/25/03 1/24/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☑ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the application papers on 17 September 2003. Claims 56-98 and 204-257 are pending; claims 1-55 and 99-203 have been cancelled.

Allowable Subject Matter

Claims 56-98 and 204-257 are allowed.

Reasons for Allowance

Referring to claims 56, 84, 204, 236 and their dependents, the following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of forming an electrical device where a first module is fabricated from a first plurality of low-temperature co-fired ceramic ("LTCC") layers, the first plurality of layers forming at least a first circuit used in the operation of the MEMS device; fabricating a second module from a second plurality of low-temperature co-fired ceramic ("LTCC") layers, the second plurality of layers forming at least a second circuit used in the operation of the MEMS device; polishing a surface of a front layer of the first module, to be used as a substrate after fabrication of the first module is completed; fabricating on the front layer the at least one MEMS device using MEMS processing; and bonding the first and second modules together to thereby form a cavity containing the at least one MEMS device.

For example, Hinds (6,225,692) discloses a method of forming an electrical device where a first module is fabricated from a first low-temperature co-fired ceramic ("LTCC") layer (30) forming at least a first circuit used in the operation of the MEMS device (10); fabricating a second module from a second low-temperature co-fired ceramic ("LTCC") layer (22) forming at least a second circuit used in the operation of the MEMS device (10) (col. 3, lines 12-51); bonding the first and second modules (30, 22) together; and forming a cavity in the first module (30) (col. 3, line 63 thru col. 4, line 11). However, Hinds does not disclose, anticipate, teach, or suggest fabricating a plurality of low-temperature co-fired ceramic ("LTCC") layers; polishing a surface of a front layer of the first module, to be used as a substrate after fabrication of the first module is completed; and bonding the first and second modules together to thereby form a cavity containing the at least one MEMS device.

Newton et al. (2002/0075651) disclose a method of forming an electrical device where a first module (21/20') is fabricated from a first plurality of low-temperature co-fired ceramic ("LTCC") layers (21a, 21b) (para. 220); fabricating a second module from a second plurality of low-temperature co-fired ceramic ("LTCC") layers; and bonding the first and second modules together (para. 38). However, Newton et al. do not disclose, anticipate, teach or suggest polishing a surface of a front layer of the first module, to be used as a substrate after fabrication of the first module is completed; fabricating on the front layer the at least one MEMS device using MEMS processing; and bonding the first and second modules together to thereby form a cavity containing the at least one MEMS device.

Peterson et al. (6,538,312) disclose a method of forming an electrical device where a first module (30') is fabricated from a first plurality of low-temperature co-fired ceramic ("LTCC") layers (67, 68, 69, 70, 71, 72), the first plurality of layers forming at least a first circuit used in the operation of the MEMS device; fabricating a second module (16') from a second plurality of low-temperature co-fired ceramic ("LTCC") layers (61, 62, 63, 64, 65, 66), the second plurality of layers forming at least a second circuit used in the operation of the MEMS device (col. 9, lines 45-52); and bonding the first and second modules (30', 16') together thereby forming a cavity containing the at least one MEMS device (100) (Fig. 3B; col. 9, lines 23-44). However, Peterson et al. do not disclose, anticipate, teach or suggest polishing a surface of a front layer of the first module, to be used as a substrate after fabrication of the first module is completed.

Referring to claim 235, the following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of forming an array antenna comprising the steps of: fabricating a plurality of radiating elements, each of the radiating elements being fabricated by forming at least one microelectromechanical ("MEMS") switch on a first low-temperature co-fired ceramic ("LTCC") module, and bonding a second LTCC bonded to the first LTCC module, whereby the MEMS switch is located in a cavity between the first and second LTCC modules; forming a plurality of sub-array modules, each of the sub-array modules being formed from a plurality of radiating elements; integrating the plurality of sub-array modules together to form the

phased array antenna; and connecting the plurality of sub-array modules to at least one amplifier.

For example, Fathy et al. (6,154,176) disclose a method of forming an array antenna where a plurality of radiating elements, each of the radiating elements (114/818) being fabricated by forming at least one microelectromechanical ("MEMS") switch (col. 11, lines 48-57), is fabricated on a first low-temperature co-fired ceramic ("LTCC") module (102/816), and bonding a second LTCC (814) to the first LTCC module (818) (col. 4, lines 45-65; col. 10, lines 49-60); forming a plurality of sub-array modules, each of the sub-array modules being formed from a plurality of radiating elements; and integrating the plurality of sub-array modules together to form the phased array antenna (col. 11, lines 36-47). However, Fathy et al. do not disclose, anticipate, teach, or suggest the MEMS switch is located in a cavity between the first and second LTCC modules; and connecting the plurality of sub-array modules to at least one amplifier.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571)

272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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